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VERILOG LANGUAGE FEATURES (PART 3)

Example Interview Questions for a job in FPGA, VHDL, Verilog

EEVblog #496 - What Is An FPGA?

Internal Block Diagram Of 8237 Dma Controller( )*Tutorial how to Write and Simulate a Verilog program in Vivado(FPGA)* Vivado Simulator and Test Bench in Verilog | Xilinx FPGA Programming Tutorials ~~Lec-3 Verilog: Part-II~~

What is an FPGA? Intro for Beginners

Full Adder - Complete Explanation and Demo with Verilog

VHDL vs. Verilog - Which Language Is Better for FPGA#7 Gate level modeling and structural modeling | explained with verilog codes *#1 Cadence SKILL Programming Tutorial for Beginners (7 lessons total) 2/16/2016*

Levels of Abstraction in Verilog

Verification Mentoring Workshop: Session 1 (Rajeev Alur, Rupak Majumdar)Mod-03 Lec-10 Concurrency, Data flow and Behavioural models *Digital Design using verilog HDL: Introduction to Digital Design and Flow: Session 1* ~~Vivado HLS Technical Introduction~~

Mod-02 Lec-06 Controller Design

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The verilog is a bit out of date althought he author does explain that newer versions have some differences. The first chapter on IN and OUT is pretty good as an introduction, several examples of combinatorial logic (although not really developing useful example).

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Verilog by Example A Concise Introduction for FPGA Design “The amount of design wins and early adoptions are ahead of wherewe expected them to be,” says Gavrielov. “We’re definitely ahead of plan in terms of yield,” adds Gavrielov,”we’re not seeing yield issues on HPL.

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Verilog by Example: A Concise Introduction for FPGA Design ...
Verilog, standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems.It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction.It is also used in the verification of analog circuits and mixed-signal circuits, as well as in the design of genetic circuits.

A practical primer for the student and practicing engineer already familiar with the basics of digital design, the reference develops a working grasp of the verilog hardware description language step-by-step using easy-to-understand examples. Starting with a simple but workable design sample, increasingly more complex fundamentals of the language are introduced until all major features of verilog are brought to light. Included in the coverage are state machines, modular design, FPGA-based memories, clock management, specialized I/O, and an introduction to techniques of simulation. The goal is to prepare the reader to design real-world FPGA solutions. All the sample code used in the book is available online. What Strunk and White did for the English language with "The Elements of Style," VERILOG BY EXAMPLE does for FPGA design.

With this book, you can: - Start writing synthesizable Verilog models quickly. - See what constructs are supported for synthesis and how these map to hardware so that you can get the desired logic. - Learn techniques to help avoid having functional mismatches. - Immediately start using many of the models for commonly used hardware elements described for your own use or modify these for your own application.

The book is divided into four major parts. Part I covers HDL constructs and synthesis of basic digital circuits. Part II provides an overview of embedded software development with the emphasis on low–level I/O access and drivers. Part III demonstrates the design and development of hardware and software for several complex I/O peripherals, including PS2 keyboard and mouse, a graphic video controller, an audio codec, and an SD (secure digital) card. Part IV provides three case studies of the integration of hardware accelerators, including a custom GCD (greatest common divisor) circuit, a Mandelbrot set fractal circuit, and an audio synthesizer based on DDFS (direct digital frequency synthesis) methodology. The book utilizes FPGA devices, Nios II soft–core processor, and development platform from Altera Co., which is one of the two main FPGA manufactures. Altera has a generous university program that provides free software and discounted prototyping boards for educational institutions (details at http://www.altera.com/university). The two main educational prototyping boards are known as DE1 ($99) and DE2 ($269). All experiments can be implemented and tested with these boards. A board combined with this book becomes a “turn–key” solution for the SoPC design experiments and projects. Most HDL and C codes in the book are device independent and can be adapted by other prototyping boards as long as a board has similar I/O configuration.

Introduction to Logic Synthesis Using Verilog HDL explains how to write accurate Verilog descriptions of digital systems that can be synthesized into digital system netlists with desirable characteristics. The book contains numerous Verilog examples that begin with simple combinational networks and progress to synchronous sequential logic systems. Common pitfalls in the development of synthesizable Verilog HDL are also discussed along with methods for avoiding them. The target audience is anyone with a basic understanding of digital logic principles who wishes to learn how to model digital systems in the Verilog HDL in a manner that also allows for automatic synthesis. A wide range of readers, from hobbyists and undergraduate students to seasoned professionals, will find this a compelling and approachable work. The book provides concise coverage of the material and includes many examples, enabling readers to quickly generate high-quality synthesizable Verilog models.

A hands-on introduction to FPGA prototyping and SoC design This is the successor edition of the popular FPGA Prototyping by Verilog Examples text. It follows the same “learning-by-doing” approach to teach the fundamentals and practices of HDL synthesis and FPGA prototyping. The new edition uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP (intellectual property) cores, integrate them into an SoC (system on a chip) framework, realize the system on an FPGA prototyping board, and verify the hardware and software operation. The examples start with simple gate-level circuits, progress gradually through the RT (register transfer) level modules, and lead to a functional embedded system with custom I/O peripherals and hardware accelerators. Although it is an introductory text, the examples are developed in a rigorous manner, and the derivations follow the strict design guidelines and coding practices used for large, complex digital systems. The book is completely updated and uses the SystemVerilog language, which “absorbs” the Verilog language. It presents the hardware design in the SoC context and introduces the hardware-software co-design concept. Instead of treating examples as isolated entities, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software “programmability” and develop complex and interesting embedded system projects. The new edition: Adds four general-purpose IP cores, which are multi-channel PWM (pulse width modulation) controller, I2C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller. Introduces a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelope generator. Expands the original video controller into a complete stream based video subsystem that incorporates a video synchronization circuit, a test-pattern generator, an OSD (on-screen display) controller, a sprite generator, and a frame buffer. Provides a detailed discussion on blocking and nonblocking statements and coding styles. Describes basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor. Provides an overview of bus interconnect and interface circuit. Presents basic embedded system software development. Suggests additional modules and peripherals for interesting and challenging projects. FPGA Prototyping by SystemVerilog Examples makes a natural companion text for introductory and advanced digital design courses and embedded system courses. It also serves as an ideal self-teaching guide for practicing engineers who wish to learn more about this emerging area of interest.

Why learn and use Verilog if you're a student, beginning designer, or leading edge systems designer? The naive would ignore Verilog and "standardize" by using VHDL, the result of a decade-long committee design process. A single language for the whole world would appear to: ease the training of designers and others who use descriptions, increase tool competition to lower costs, and increase design sharing and library usage. Further, the U. S. Department of Defense (DOD) mandated its use for design description Mandated standards rarely are best, and often not very good. Competition is good because it encourages rapid evolution. Also, we know that evolved, de facto standards embodied in a time-tested product based on initial conceptual clarity from one person or organization versus de jure standards coming from large committees or government mandates are often preferred. A standard must be "open" so that many others can use it, build on it, and compete to make it better. One only has to compare: C, C++, and FORTRAN versus ADA (DOD's mandated language), PLl; TCP/IP versus OSI; the Intel X86 or PowerPC microprocessors versus DOD's many architectures; Windows versus the many UNIX dialects; and various industry buses versus DOD's Futurebus. Verilog, introduced in 1985, was developed by one person, Phil Moorby at Gate way Design Automation. It was Phil's third commercial logic simulator.

A practical primer for the student and practicing engineer already familiar with the basics of digital design, the reference develops a working grasp of the VHLD hardware description language step-by-step using easy-to-understand examples. Starting with a simple but workable design sample, increasingly more complex fundamentals of the language are introduced until all core features of VHDL are brought to light. Included in the coverage are state machines, modular design, FPGA-based memories, clock management, specialized I/O, and an introduction to techniques of simulation. The goal is to prepare the reader to design real-world FPGA solutions. All the sample code used in the book is available online. What Strunk and White did for the English language with "The Elements of Style," VHDL BY EXAMPLE does for FPGA design.

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real-world experience.

Designing a complex ASIC/SoC is similar to learning a new language to start with and ultimately creating a masterpiece using experience, imagination, and creativity. Digital design starts with RTL such as Verilog or VHDL, but it is only the beginning. A complete designer needs to have a good understanding of the Verilog language, digital design techniques, system architecture, IO protocols, and hardware-software interaction. Some of it will come from experience, and some will come with concerted effort. Graduating from college and entering into the world of digital system design becomes an overwhelming task, as not all the information is readily available. In this book, we have made an effort to explain the concepts in a simple way with real-world examples in Verilog. The book is intended for digital and system design engineers with emphasis on design and system architecture. The book is broadly divided into two sections - chapters 1 through 10, focusing on the digital design aspects and chapters 11 through 20, focusing on the system aspects of chip design. This book can be used by students taking digital design and chip design courses in college and availing it as a guide in their professional careers. Chapter 3 focuses on the synthesizable Verilog constructs, with examples on reusable design (parameterized design, functions, and generate structure). Chapter 5 describes the basic concepts in digital design - logic gates, truth table, De Morgan's theorem, set-up and hold time, edge detection, and number system. Chapter 6 goes into details of digital design explaining larger building blocks such as LFSR, scrambler/descramblers, error detection and correction, parity, CRC, Gray encoding/decoding, priority encoders, 8b/10b encoding, data converters, and synchronization techniques. Chapter 7 and 8 bring in advanced concepts in chip design and architecture - clocking and reset strategy, methods to increase throughput and reduce latency, flow-control mechanisms, pipeline operation, out-of-order execution, FIFO design, state machine design, arbitration, bus interfaces, linked list structure, and LRU usage and implementation. Chapter 9 and 10 describe how to build and design ASIC/SoC. It talks about chip micro-architecture, portioning, datapath, control logic design, and other aspects of chip design such as clock tree, reset tree, and EEPROM. It also covers good design practices, things to avoid and adopt, and best practices for high-speed design. The second part of the book is devoted to System architecture, design, and IO protocols. Chapter 11 talks about memory, memory hierarchy, cache, interrupt, types of DMA and DMA operation. There is Verilog RTL for a typical DMA controller design that explains the scatter-gather DMA concept. Chapter12 describes hard drive, solid-state drive, DDR operation, and other parts of a system such as BIOS, OS, drivers, and their interaction with hardware. Chapter 13 describes embedded systems and internal buses such as AHB, AXI used in embedded design. It describes the concept of transparent and non-transparent bridging. Chapter 14 and chapter 15 bring in practical aspects of chip development - testing, DFT, scan, ATPG, and detailed flow of the chip development cycle (Synthesis, Static timing, and ECO). Chapter 16 and chapter 17 are on power saving and power management protocols. Chapter 16 has a detailed description of various power savings techniques (frequency variation, clock gating, and power well isolation). Chapter 17 talks about Power Management protocols such as system S states, CPU C states, and device D states. Chapter 18 explains the architecture behind serial-bus technology, PCS, and PMA layer. It describes clocking architecture and advanced concepts such as elasticity FIFO, channel bonding (deskewing), link aggregation, and lane reversal. Chapter 19 and 20 are devoted to serial bus protocols (PCI Express, Serial ATA, USB, Thunderbolt, and Ethernet) and their operation.

Field Programmable Gate Arrays (FPGAs) are devices that provide a fast, low-cost way for embedded system designers to customize products and deliver new versions with upgraded features, because they can handle very complicated functions, and be reconfigured an infinite number of times. In addition to introducing the various architectural features available in the latest generation of FPGAs, The Design Warrior’s Guide to FPGAs also covers different design tools and flows. This book covers information ranging from schematic-driven entry, through traditional HDL/RTL-based simulation and logic synthesis, all the way up to the current state-of-the-art in pure C/C++ design capture and synthesis technology. Also discussed are specialist areas such as mixed hardward/software and DSP-based design flows, along with innovative new devices such as field programmable node arrays (FPNAs). Clive "Max" Maxfield is a bestselling author and engineer with a large following in the electronic design automation (EDA)and embedded systems industry. In this comprehensive book, he covers all the issues of interest to designers working with, or contemplating a move to, FPGAs in their product designs. While other books cover fragments of FPGA technology or applications this is the first to focus exclusively and comprehensively on FPGA use for embedded systems. First book to focus exclusively and comprehensively on FPGA use in embedded designs World-renowned best-selling author Will help engineers get familiar and succeed with this new technology by providing much-needed advice on choosing the right FPGA for any design project